

Abstract

Systems, methods and devices for scrambling/descrambling sets of data bits using subsets of a recurring sequence of scrambler bits. A self-synchronous scrambler, regardless of the generating polynomial being implemented, will generate repeating sequences of scrambler bits regardless of the initial stage of the scrambler. To implement a parallel scrambler, given a current state of the scrambler, the next n states of the scrambler are predicted based on the current state of the scrambler. The scrambling operation can then be preformed using the values in the current state - parallel logic operations between preselected bits of the current state will yield the required values to be used in scrambling an incoming parallel data set. Once these required values are generated, a parallel logical operation between the required values and the incoming data set will result in the scrambled output data. The current state of the scrambler is then incremented by n_{+1} by performing a predetermined set of logical operations between the various bits of the current state such that each bit of the n_{+1} state is a result of a logical operation between selected and predetermined bits of the current state.